



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Farnworth et. al.

Serial No.: 10/690,496

Filed: October 21, 2003

For: DEVICE AND METHOD FOR
ISOLATING A SHORT-CIRCUITED
INTEGRATED CIRCUIT (IC) FROM
OTHER IC'S ON A SEMICONDUCTOR
WAFER

Confirmation No.: 5053

Examiner: Minh Nhut Tang

Group Art Unit: 2829

Attorney Docket No.: 2269-3038.3US
(96-0936.03/US)

Notice of Allowance Mailed:

August 9, 2004

Express Mail Mailing Label No.: EL 994821965 US

Date of Deposit with USPS: October 29, 2004

Person making Deposit: Christopher Haughton

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of \$1,685.00 in payment therefor plus five (5) copies of the patent when issued.

Serial No.: 10/690,496

Also, enclosed are Comments on Statement of Reasons for Allowance (2 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,



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Attorney for Applicant(s)
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Salt Lake City, Utah 84110-2550
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Date: October 29, 2004
JRD/ps:dh

Enclosures: Part B - Issue Fee Transmittal
Check No. 21043 in the amount of \$1,685.00
Copy of Transmittal Letter
Comments on Statement of Reasons for Allowance (2 pages)
Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)

Document in ProLaw



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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates:

Claims 1-13 recite, inter alia, an integrated circuit having an internal circuit and an external terminal for communicating between the internal circuit and circuitry external to the integrated circuit, the external terminal for receiving a

supply voltage from the circuitry external to the integrated circuit, comprising a device for isolating the internal circuit from the external terminal, the device having control circuitry for sensing a short in the internal circuit and outputting a control signal in response thereto, the control circuitry including circuitry for sensing current drawn by the internal circuit exceeding a predetermined threshold and for outputting the control signal in response thereto, the control circuitry including a first transistor having a source coupled to a supply terminal, a gate coupled to an output terminal, and a drain coupled to a control signal terminal; a first resistive device coupled between the supply terminal and the output terminal; a second resistive device coupled between the control signal terminal and a reference voltage bond pad; a second transistor having a source coupled to the supply terminal, a gate, and a drain coupled to the control signal terminal; and an inverter coupled between the control signal terminal and the gate of the second transistor; and circuitry for sensing the voltage applied to the internal circuit.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,



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